

# NTS0104-Q100

Dual supply translating transceiver; open drain; auto direction sensing

Rev. 3 — 7 August 2012

Product data sheet

## 1. General description

The NTS0104-Q100 is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied with any voltage between 1.65 V and 3.6 V.  $V_{CC(B)}$  can be supplied with any voltage between 2.3 V and 5.5 V. The range in supply voltages makes the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 1.65 V to 3.6 V and  $V_{CC(B)}$ : 2.3 V to 5.5 V
- Maximum data rates:
  - ◆ Push-pull: 50 Mbps
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - ◆ MIL-STD-883, method 3015 Class 2 exceeds 2500 V for A port
  - ◆ MIL-STD-883, method 3015 Class 3B exceeds 15000 V for B port
  - ◆ HBM JESD22-A114E Class 2 exceeds 2500 V for A port
  - ◆ HBM JESD22-A114E Class 3B exceeds 15000 V for B port
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options



### 3. Applications

- I<sup>2</sup>C/SMBus
- UART
- GPIO

### 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NTS0104UK-Q100	-40 °C to +125 °C	WLCSP12	wafer level chip scale package; 12 balls; 1.2 × 1.6 × 0.56 mm	NTS0104UK-Q100

### 5. Marking

Table 2. Marking

Type number	Marking code
NTS0104UK-Q100	s04

### 6. Functional diagram

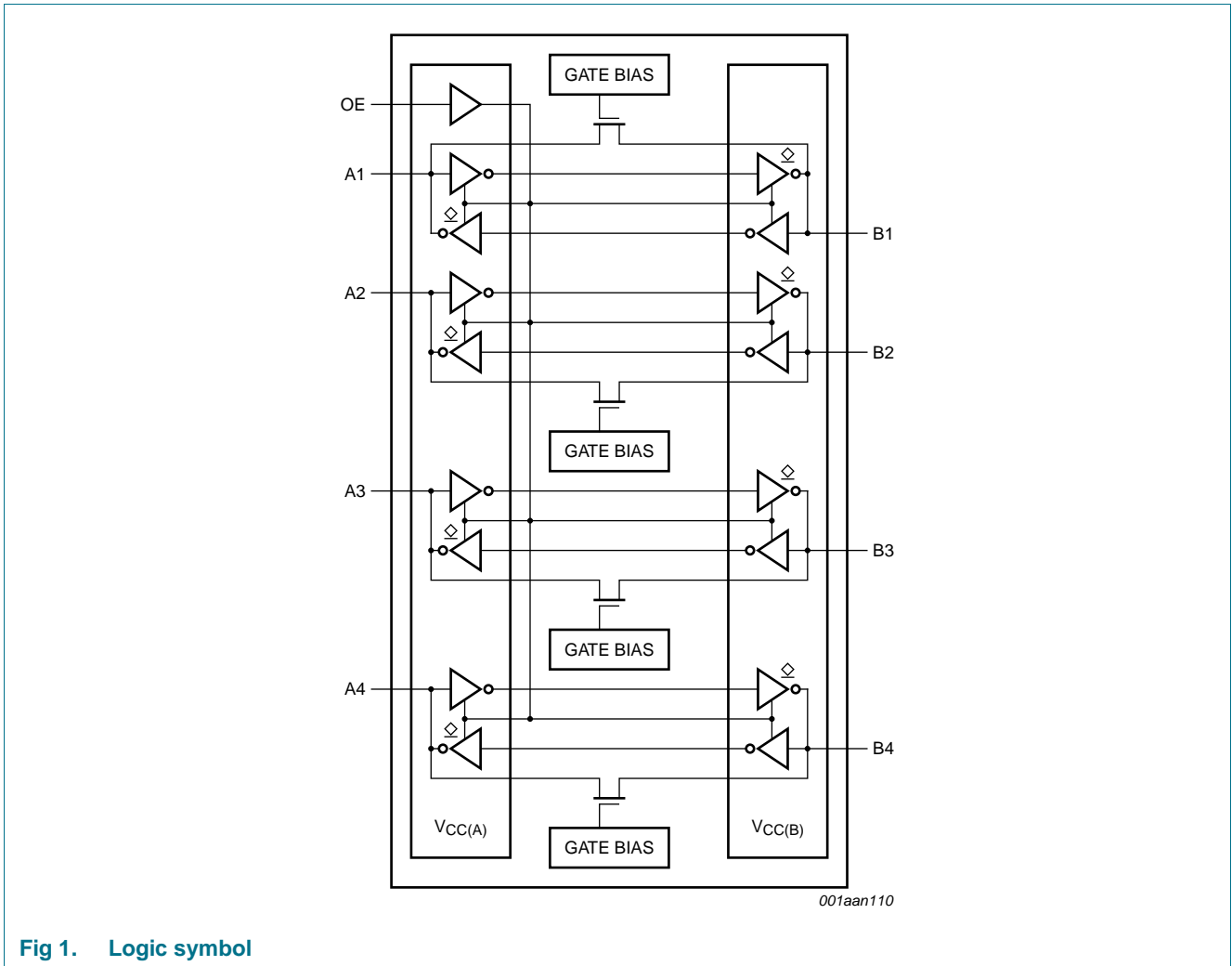


Fig 1. Logic symbol

## 7. Pinning information

### 7.1 Pinning

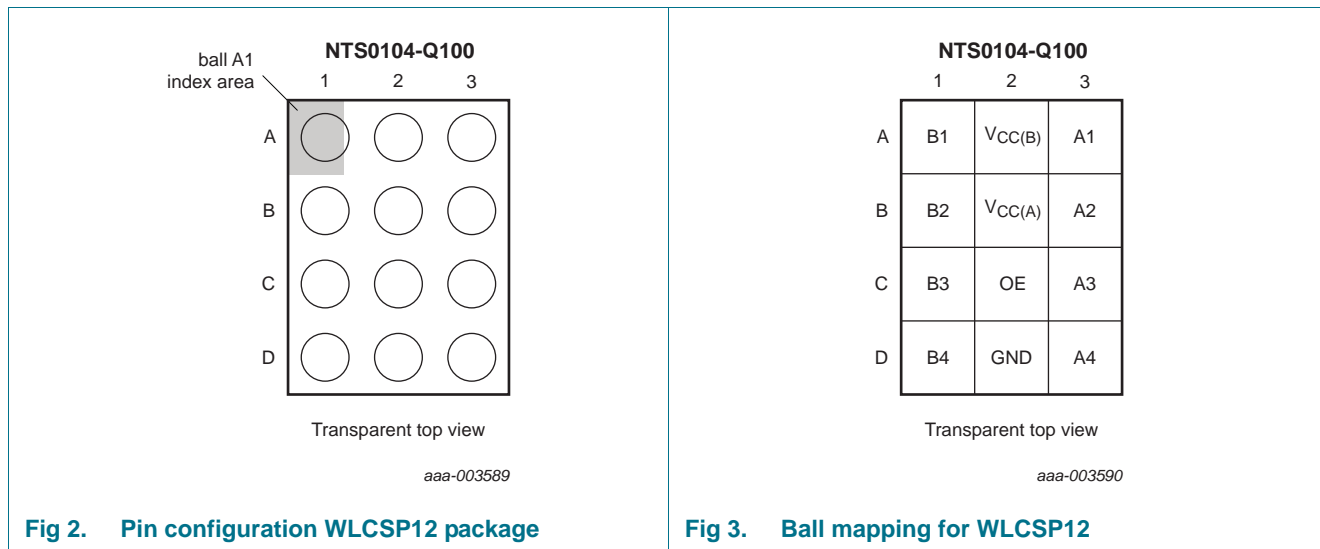


Fig 2. Pin configuration WLCSP12 package

Fig 3. Ball mapping for WLCSP12

### 7.2 Pin description

Table 3. Pin description

Symbol	Ball	Description
V <sub>CC(A)</sub>	B2	supply voltage A
A1, A2, A3, A4	A3, B3, C3, D3	data input or output (referenced to V <sub>CC(A)</sub> )
n.c.	-	not connected
GND	D2	ground (0 V)
OE	C2	output enable input (active HIGH; referenced to V <sub>CC(A)</sub> )
B4, B3, B2, B1	D1, C1, B1, A1	data input or output (referenced to V <sub>CC(B)</sub> )
V <sub>CC(B)</sub>	A2	supply voltage B

## 8. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage		Input	Input/output	
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	OE	An	Bn
1.65 V to V <sub>CC(B)</sub>	2.3 V to 5.5 V	L	Z	Z
1.65 V to V <sub>CC(B)</sub>	2.3 V to 5.5 V	H	input or output	output or input
GND <sup>[2]</sup>	GND <sup>[2]</sup>	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into power-down mode.

## 9. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V	
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V	
$V_I$	input voltage	A port and OE input	[1][2]	-0.5	+6.5	V
		B port	[1][2]	-0.5	+6.5	V
$V_O$	output voltage	Active mode	[1][2]			
		A or B port	-0.5	$V_{CCO} + 0.5$	V	
		Power-down or 3-state mode	[1]			
		A port	-0.5	+4.6	V	
		B port	-0.5	+6.5	V	
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA	
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA	
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	[2]	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA	
$I_{GND}$	ground current		-100	-	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	250	mW	

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

## 10. Recommended operating conditions

**Table 6. Recommended operating conditions**[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V

[1] Hold the A and B sides of an unused I/O pair in the same state, either both at  $V_{CC1}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

## 11. Static characteristics

**Table 7. Typical static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	[1]	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }5.5\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	2	-	pF
$C_{I/O}$	input/output capacitance	A port	-	4	-	pF
		B port	-	7	-	pF
		A or B port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	9	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output.

**Table 8. Typical supply current**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	$\mu\text{A}$
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	$\mu\text{A}$
3.3 V	-	-	0.1	0.1	0.1	2.8	$\mu\text{A}$

**Table 9. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Max	Min	Max		
$V_{IH}$	HIGH-level input voltage	A port						
		$V_{CC(A)} = 1.65\text{ V to }1.95\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.2$	-	$V_{CCI} - 0.2$	-	V
		$V_{CC(A)} = 2.3\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		B port						
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		OE input						
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$		$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V

**Table 9. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IL</sub>	LOW-level input voltage	A or B port V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.15	-	0.15	V
		OE input V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	A or B port; I <sub>O</sub> = -20 μA V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	[2] 0.67V <sub>CCO</sub>	-	0.67V <sub>CCO</sub>	-	V
V <sub>OL</sub>	LOW-level output voltage	A or B port; I <sub>O</sub> = 1 mA V <sub>I</sub> ≤ 0.15 V; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	[2]	-	0.4	-	0.4 V
I <sub>I</sub>	input leakage current	OE input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	[2]	-	±2	-	±12 μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0 V to 5.5 V	-	±2	-	±12	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0 V to 3.6 V	-	±2	-	±12	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A	[1]				
		I <sub>CC(A)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	2.4	-	15	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2.2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-1	-	-8	μA
		I <sub>CC(B)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	12	-	30	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-1	-	-5	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	1	-	6	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub> V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	14.4	-	45	μA

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

## 12. Dynamic characteristics

**Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C<sup>[1]</sup>**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.8 V ± 0.15 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	4.6	-	4.7	-	5.8	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	6.8	-	6.8	-	7.0	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <a href="#">[2]</a>	-	35	-	35	-	35	ns
		OE to B; no external load <a href="#">[2]</a>	-	35	-	35	-	35	ns
		OE to A	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
t <sub>sk(o)</sub>	output skew time	between channels <a href="#">[3]</a>	-	0.7	-	0.7	-	0.7	ns
t <sub>w</sub>	pulse width	data inputs	20	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	50	-	50	-	50	Mbps
<b>V<sub>CC(A)</sub> = 2.5 V ± 0.2 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	3.2	-	3.3	-	3.4	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	3.5	-	4.1	-	4.4	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	0.7	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <a href="#">[2]</a>	-	35	-	35	-	35	ns
		OE to B; no external load <a href="#">[2]</a>	-	35	-	35	-	35	ns
		OE to A	-	200	-	200	-	200	ns
		OE to B	-	200	-	200	-	200	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	2.8	7.4	2.6	6.6	1.8	6.2	ns
		B port	3.2	8.3	2.9	7.9	2.4	6.8	ns



**Table 10. Dynamic characteristics for temperature range –40 °C to +85 °C<sup>[1]</sup>**

*Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#).*

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t <sub>THL</sub>	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
t <sub>sk(o)</sub>	output skew time	between channels <sup>[3]</sup>	-	0.7	-	0.7	-	0.7	ns
t <sub>W</sub>	pulse width	data inputs	20	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	50	-	50	-	50	Mbps
<b>V<sub>CC(A)</sub> = 3.3 V ± 0.3 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
t <sub>en</sub>	enable time	OE to A; B	-	-	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <sup>[2]</sup>	-	-	-	35	-	35	ns
		OE to B; no external load <sup>[2]</sup>	-	-	-	35	-	35	ns
		OE to A	-	-	-	260	-	260	ns
		OE to B	-	-	-	200	-	200	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	-	-	2.3	5.6	1.9	5.9	ns
		B port	-	-	2.5	6.4	2.1	7.4	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
t <sub>sk(o)</sub>	output skew time	between channels <sup>[3]</sup>	-	-	-	0.7	-	0.7	ns
t <sub>W</sub>	pulse width	data inputs	-	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	-	-	50	-	50	Mbps

[1] t<sub>en</sub> is the same as t<sub>pZL</sub> and t<sub>pZH</sub>.

t<sub>dis</sub> is the same as t<sub>pLZ</sub> and t<sub>pHZ</sub>.

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

**Table 11. Dynamic characteristics for temperature range –40 °C to +125 °C<sup>[1]</sup>**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#).

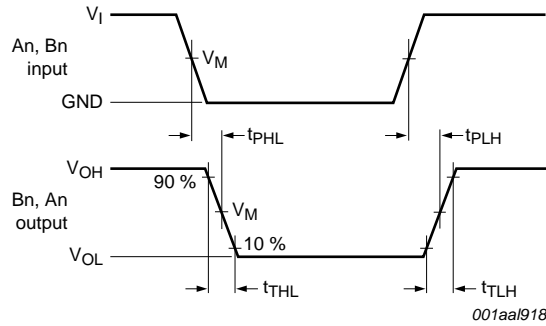
Symbol	Parameter	Conditions	V <sub>CC(B)</sub>						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
<b>V<sub>CC(A)</sub> = 1.8 V ± 0.15 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <sup>[2]</sup>	-	45	-	45	-	45	ns
		OE to B; no external load <sup>[2]</sup>	-	45	-	45	-	45	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t <sub>THL</sub>	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
t <sub>sk(o)</sub>	output skew time	between channels <sup>[3]</sup>	-	0.8	-	0.8	-	0.8	ns
t <sub>W</sub>	pulse width	data inputs	20	-	20	-	20	-	ns
f <sub>data</sub>	data rate		-	50	-	50	-	50	Mbps
<b>V<sub>CC(A)</sub> = 2.5 V ± 0.2 V</b>									
t <sub>PHL</sub>	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
t <sub>en</sub>	enable time	OE to A; B	-	200	-	200	-	200	ns
t <sub>dis</sub>	disable time	OE to A; no external load <sup>[2]</sup>	-	45	-	45	-	45	ns
		OE to B; no external load <sup>[2]</sup>	-	45	-	45	-	45	ns
		OE to A	-	220	-	220	-	220	ns
		OE to B	-	220	-	220	-	220	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns

**Table 11. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ <sup>[1]</sup> ...continued**  
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#); for wave forms see [Figure 4](#) and [Figure 5](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$t_{THL}$	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
$t_{sk(o)}$	output skew time	between channels <sup>[3]</sup>	-	0.8	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs	20	-	20	-	20	-	ns
$f_{data}$	data rate		-	50	-	50	-	50	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
$t_{en}$	enable time	OE to A; B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <sup>[2]</sup>	-	-	-	45	-	45	ns
		OE to B; no external load <sup>[2]</sup>	-	-	-	45	-	45	ns
		OE to A	-	-	-	280	-	280	ns
		OE to B	-	-	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	7.0	1.9	7.4	ns
		B port	-	-	2.5	8.0	2.1	9.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	6.8	1.9	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
$t_{sk(o)}$	output skew time	between channels <sup>[3]</sup>	-	-	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs	-	-	20	-	20	-	ns
$f_{data}$	data rate		-	-	-	50	-	50	Mbps

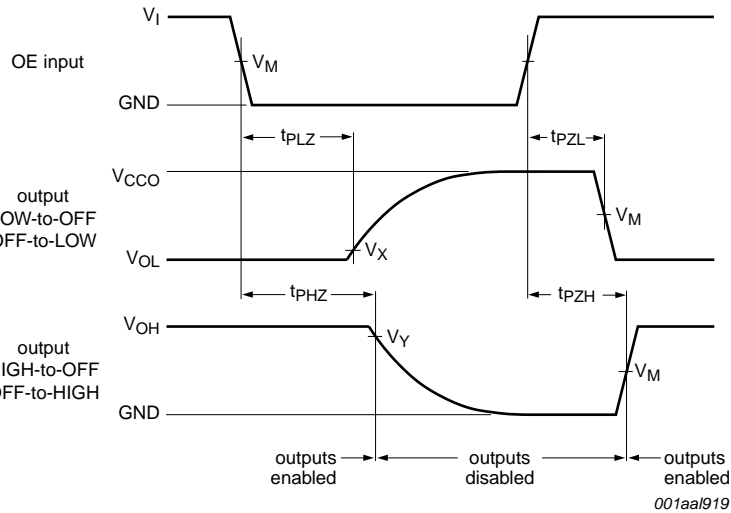
[1]  $t_{en}$  is the same as  $t_{pZL}$  and  $t_{pZH}$ .  
 $t_{dis}$  is the same as  $t_{pLZ}$  and  $t_{pHZ}$ .  
 [2] Delay between OE going LOW and when the outputs are disabled.  
 [3] Skew between any two outputs of the same package switching in the same direction.

13. Waveforms



Measurement points are given in [Table 12](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 4. The data input (An, Bn) to data output (Bn, An) propagation delay times



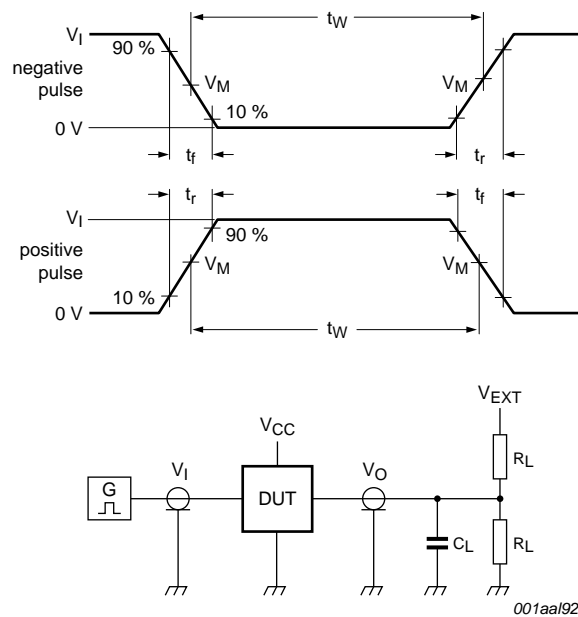
Measurement points are given in [Table 12](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 5. Enable and disable times

Table 12. Measurement points<sup>[1][2]</sup>

Supply voltage	Input	Output		
$V_{CCO}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.8 V ± 0.15 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.5 V ± 0.2 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.3 V ± 0.3 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
5.0 V ± 0.5 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1]  $V_{CCI}$  is the supply voltage associated with the input.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output.



Test data is given in [Table 13](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>O</sub> = 50 Ω; dV/dt ≥ 1.0 V/ns.

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

V<sub>EXT</sub> = External voltage for measuring switching times.

**Fig 6. Test circuit for measuring switching times**

**Table 13. Test data**

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	V <sub>I</sub> <sup>[1]</sup>	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> <sup>[2]</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> <sup>[3]</sup>
1.65 V to 3.6 V	2.3 V to 5.5 V	V <sub>CCI</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub>

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ. For measuring enable and disable times, R<sub>L</sub> = 50 kΩ.

[3] V<sub>CCO</sub> is the supply voltage associated with the output.

## 14. Application information

### 14.1 Applications

Voltage level-translation applications. The NTS0104-Q100 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I<sup>2</sup>C or 1-wire which use open-drain drivers. Although it may also be used in applications where push-pull drivers are connected to the ports, the NTB0104-Q100 may be more suitable.

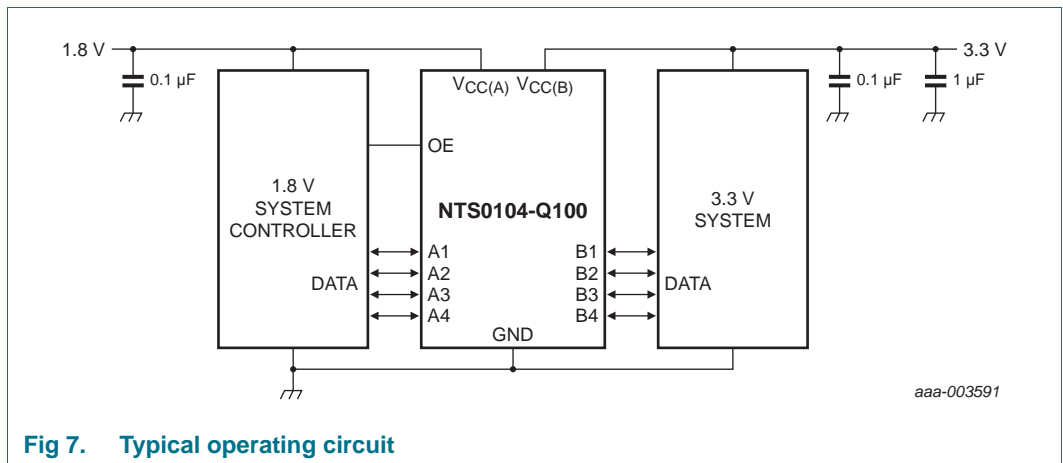


Fig 7. Typical operating circuit

### 14.2 Architecture

The architecture of the NTS0104-Q100 is shown in Figure 8. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

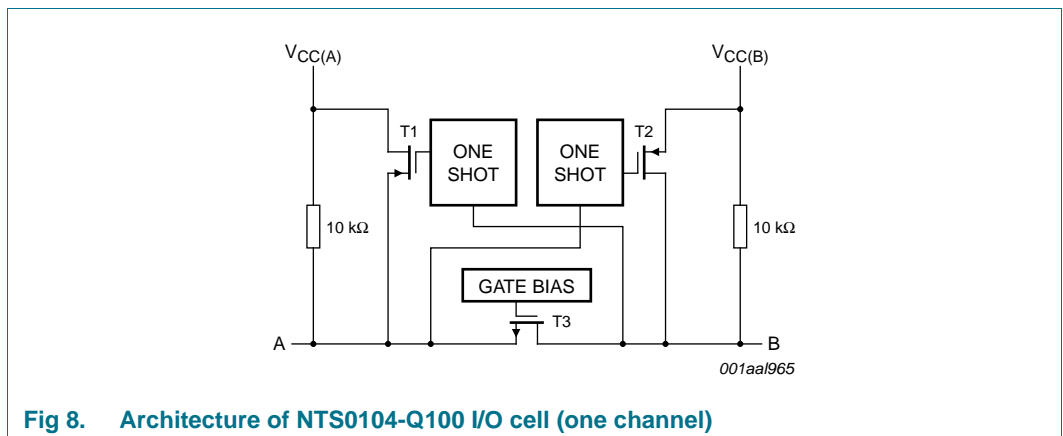


Fig 8. Architecture of NTS0104-Q100 I/O cell (one channel)

The NTS0104-Q100 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the  $V_{CC}$  level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition. This acceleration is achieved by switching on the PMOS transistors (T1, T2) bypassing the 10 k $\Omega$  pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately  $V_{CC}/2$ ; it is de-activated approximately 50 ns after the output reaches  $V_{CCO}/2$ . During the acceleration time, the driver output resistance is between approximately 50  $\Omega$  and 70  $\Omega$ . To avoid signal contention and minimize dynamic  $I_{CC}$ , wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

### 14.3 Input driver requirements

As the NTS0104-Q100 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O, determines the static current sinking capability of the system. The maximum data rate, HIGH-to-LOW output transition time ( $t_{THL}$ ) and propagation delay ( $t_{PHL}$ ), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50  $\Omega$  is used.

### 14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0104-Q100 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot retriggering, control the length of the PCB trace. The PCB trace must limit the round-trip delay of any reflection to within the one-shot pulse duration (approximately 50 ns).

### 14.5 Power-up

During operation  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ . However, during power-up  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device. This means that either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0104-Q100 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 14.6 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time required for one one-shot circuit to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, tie pin OE to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

### 14.7 Pull-up or pull-down resistors on I/Os lines

Each A port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(A)}$ . Each B port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(B)}$ . If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 k $\Omega$ . The smaller value, affects the  $V_{OL}$  level. When OE goes LOW, the internal pull-ups of the NTS0104-Q100 are disabled.



15. Package outline

WLCSP12: wafer level chip-size package,  
12 bumps; body 1.20 x 1.60 x 0.56 mm. (Backside Coating included)

NTS0104-Q100UK

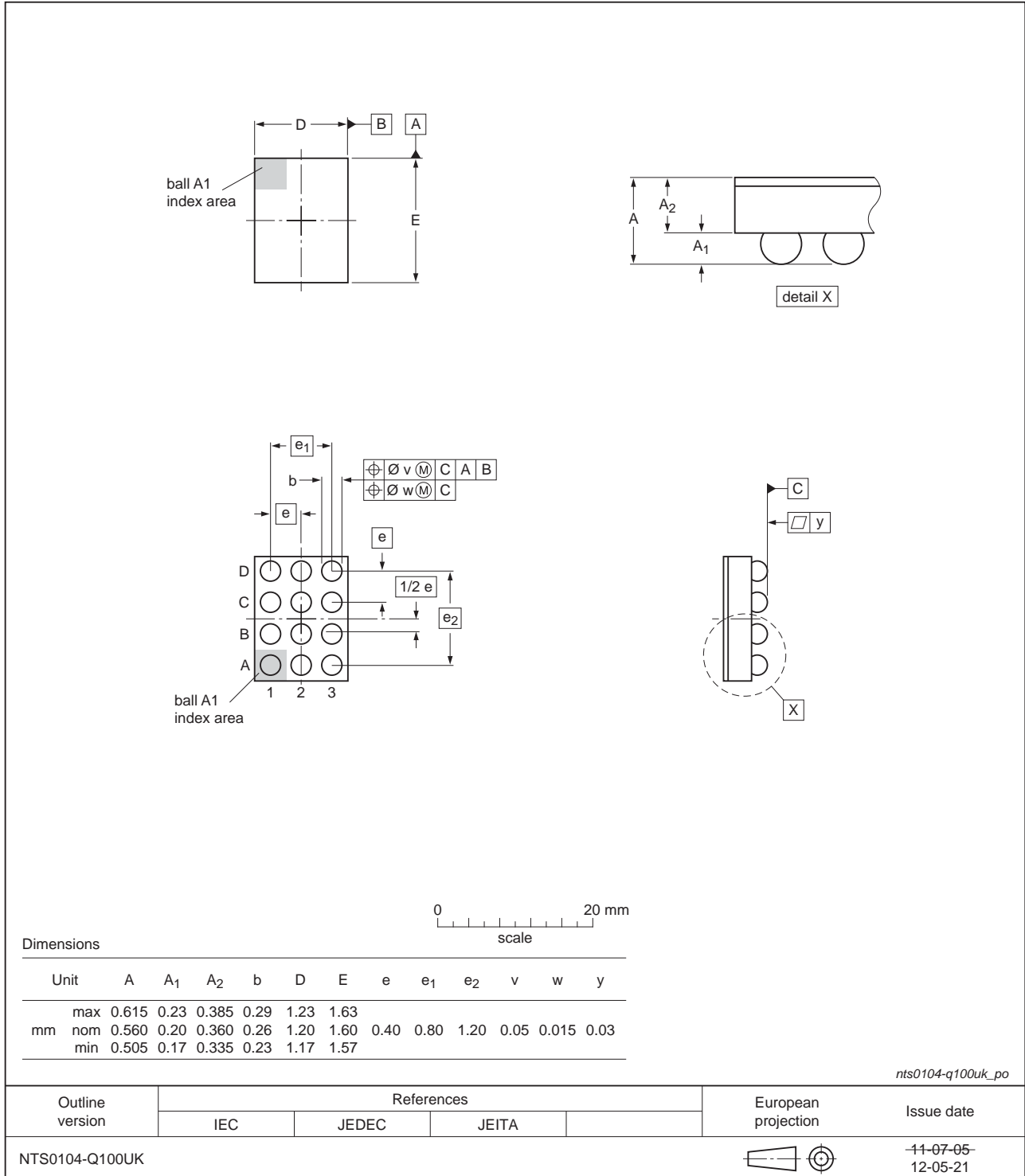


Fig 9. Package outline WLCSP12 package

## 16. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
MM	Machine Model
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter

## 17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0104_Q100 v.1	20120807	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

1 General description . . . . . 1

2 Features and benefits . . . . . 1

3 Applications . . . . . 2

4 Ordering information . . . . . 2

5 Marking . . . . . 2

6 Functional diagram . . . . . 3

7 Pinning information . . . . . 4

7.1 Pinning . . . . . 4

7.2 Pin description . . . . . 4

8 Functional description . . . . . 4

9 Limiting values . . . . . 5

10 Recommended operating conditions . . . . . 5

11 Static characteristics . . . . . 6

12 Dynamic characteristics . . . . . 8

13 Waveforms . . . . . 12

14 Application information . . . . . 14

14.1 Applications . . . . . 14

14.2 Architecture . . . . . 14

14.3 Input driver requirements . . . . . 15

14.4 Output load considerations . . . . . 15

14.5 Power-up . . . . . 15

14.6 Enable and disable . . . . . 15

14.7 Pull-up or pull-down resistors on I/Os lines . . 16

15 Package outline . . . . . 17

16 Abbreviations . . . . . 18

17 Revision history . . . . . 18

18 Legal information . . . . . 19

18.1 Data sheet status . . . . . 19

18.2 Definitions . . . . . 19

18.3 Disclaimers . . . . . 19

18.4 Trademarks . . . . . 20

19 Contact information . . . . . 20

20 Contents . . . . . 21

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